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Design of a two-stage Broadband Stable Power Amplifier for Low Power Wireless Telemetry Systems using 90 nm CMOS Technology

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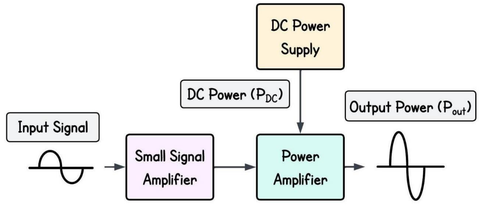
ABSTRACT & INTRODUCTION

This research offers a two-stage Power Amplifier (PA) with high gain and excellent energy efficiency using 90 nm CMOS technology in Cadence Virtuoso for wireless biomedical telemetry. It has sparked substantial attention due to its ability to enhance weak signals. Targeting the 0.9–1.25 GHz range, it uses a Common-Gate (CG) input and Common-Source (CS) output with superimposed staggered tuning. It offers optimal performance, simplicity, scalability and CMOS compatibility with 21.90 dB gain at peak. The amplifier consumes 153.1 mW power and maintains stability with with Kf > 1 and B1f > 0. Its architecture ensures low power, high efficiency, and reliable signal transmission for patient monitoring applications.



OBJECTIVES

- Design a power amplifier for high frequency.
- Design input and output matching network for impedance matching.
- Design an a CG-CS amplifier for higher gain in Telemetry system.
- Analyze the performance of the proposed amplifier for wireless biomedical application.
- Design a stable PA to avoid parasitic oscillations.

METHODOLOGY

Design Topology

- **Architecture:** 2-stage CG-CS PA.
- **1st stage:** CG with resistive load.
- **2nd stages:** CS with inductive loads for better high-frequency performance.
- **Matching Network:** T network to ensure impedance matching to 50 Ω.
- **Biasing:** Current mirror biasing and diode-connected MOS for stability and linearity.

Performance Goal

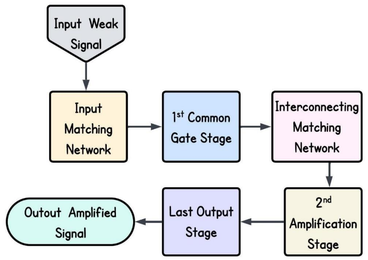
- **Gain:** High (>20 dB).
- **Stability:** Unconditionally Stable (Kf >1 & B1f > 0).
- **Power Consumption:** ~ 154mW.

Technology & Tools

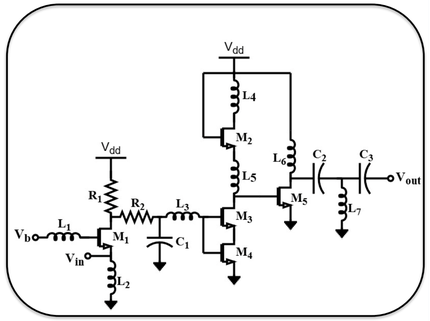
- **Process Node:** 90 nm CMOS.
- **Simulation Tool:** Cadence Virtuoso.
- **Application Target:** Telemetry System.

Special Design Features

- **Source Degeneration:** Inductor used at the source improves stability and linearity.
- **Component Optimization:** Capacitors, inductors, and transistors fine-tuned for target bandwidth.



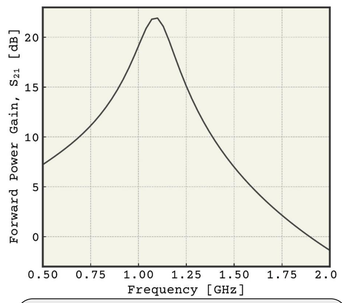
Block Diagram of the proposed PA



Schematic Diagram of the proposed PA

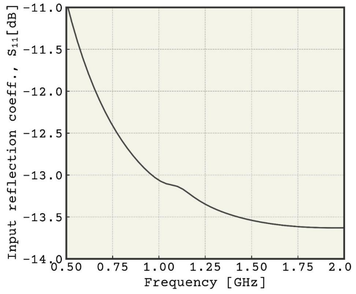
RESULT

Forward Transmission Coefficient



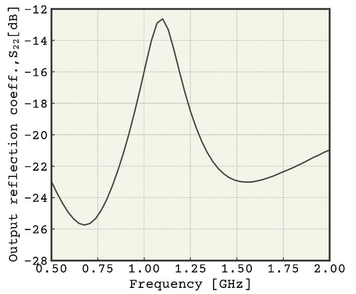
- Indicates larger gain & Strong Amplification.
- Output power is more than 100 times larger than the input power.

Input Reflection Coefficient



- Indicates how well the input is matched to the load.
- Minor amount of input power is reflected back at input port.

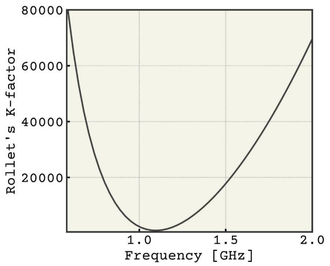
Output Reflection Coefficient



- Indicates how well the output is matched to the load.
- Minor amount of output power is reflected back at output port.

RESULT

Stability Factor



- Determines if the amplifier is unconditionally stable.
- Kf > 1 indicates unconditional stability.

CONCLUSION

This work explored the design and optimization of a PA operating within the 0.9–1.25 GHz frequency range, aiming for improved gain, bandwidth, and impedance matching. The cascaded PA outperforms the single-stage design by delivering better gain and reduced return loss with the help of matching networks. The results meet design objectives successfully by the optimization efforts, and future work will involve layout design, fabrication, and real-world validation.

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