2025 International Conference on Quantum Photonics, Artificial Intelligence, and Networking (QPAIN)
31 July – 2 August 2025, Rangpur, Bangladesh

Design of a two-stage Broadband Stable Power Amplifier for Low Power Wireless Telemetry Systems using 90 nm CMOS Technology

Nishat Anjumane Salsabila
Department of Electrical and Electronic Engineering
Chittagong University of Engineering and Technology (CUET)
Chattogram, Bangladesh
Email: nishatanjumane@gmail.com

***Abstract*—This paper presents the design of a 0.9-1.25 GHz two-stage power amplifier using 90 nm CMOS Cadence Virtuoso for a wireless telemetry system. The system utilizes radio-frequency (RF) communication to remotely measure and transmit data for monitoring patients vital signs (pulse and respiration). The design aims to balance low power consumption with performance parameters (gain, efficiency, output power, linearity, bandwidth, and thermal stability). The proposed amplifier consists of two stages, achieving strong impedance matching with S_{11} = -13.14 dB and S_{22} = -12.66 dB. It provides a forward transmission coefficient (S_{21}) of 21.90 dB to a 50 Ω load at an operating frequency of 1.097 GHz with a supply voltage of 1.2 V. Within the specified bandwidth, the gain is more significant than 15 dB. Total power consumption is 153.1 mW. The amplifier exhibits a Gain–Bandwidth Product of 18.06 dB.GHz, which is a standard metric indicating its gain-versus-bandwidth trade-off. The stability factors ($Kf > 1$ & $B1f > 0$) confirm the unconditional stability. The design successfully meets the specified requirements for the intended wireless biomedical telemetry application.**

***Index Terms*—Power amplifier, Stability factor, Wireless Telemetry, Power consumption, Bodway Factor.**

I. Introduction

An electronic device intended to boost an electrical signal's strength is called a power amplifier (PA). Wireless communication systems, radio receivers, and audio systems are just a few of the various uses for PAs. With the growing demand for higher data rates, improved signal integrity, and reduced power consumption, particularly in applications such as wireless communications, audio processing, and radar systems, the design of efficient and high-performance PAs has become critically important. The input signal's power is raised sufficiently in the PA. A PA is the last link in an amplifier chain and is made to drive loads directly, in contrast to voltage/current amplifiers. The basic signal flow and functional components of a PA system are illustrated in Fig.1, where a small-signal amplifier is followed by a PA driven by a DC supply to generate RF output.

Since one of the transistor nodes is AC grounded, there are three possible configurations for the single transistor arrangement that is typically used to create PAs. Fig.2 illustrates these

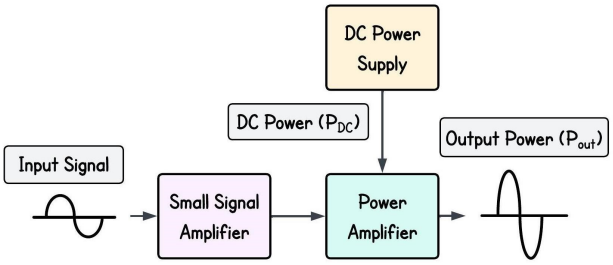


Fig. 1: Signal flow of a Power Amplifier system

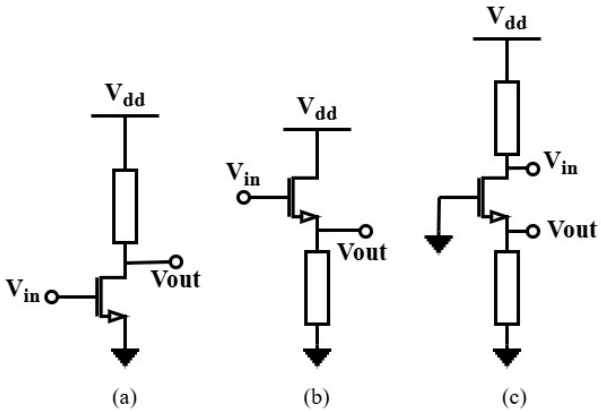
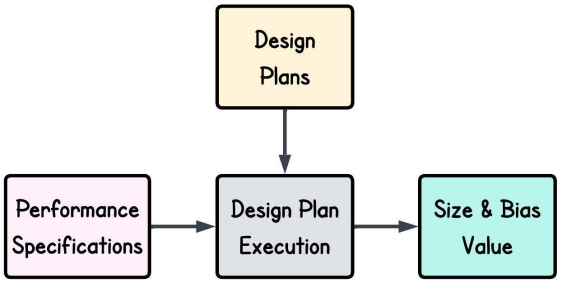


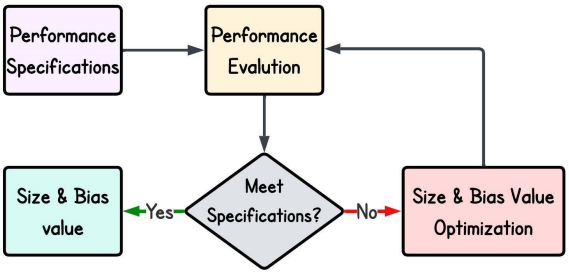
Fig. 2: Single transistor amplifier (a) Common Source; (b) Common drain; (c) Common Gate

options highlighting their input, output, and supply connections. PAs are designed to deliver high efficiency, reliability, and performance across a variety of operating conditions. Tailored to the specific application needs, different topologies and configurations are used to optimize the factors (efficiency, linearity, gain flatness, and output power). Transistor-based PAs are widely used due to their versatility and effectiveness in meeting diverse requirements. However, several challenges arise in the design and operation of PAs. For instance, two-stage op-amps limit the gain and output voltage swing, which impacts performance and reduces the unity gain bandwidth [1].

979-8-3315-9694-1/25/$31.00 ©2025 IEEE



(a)



(b)

Fig. 3: Fig. 3. Synthesis of the analog circuit (a) on knowledge, (b) on optimization.

Additionally, extra components of matching circuits reduce the gain flatness, and parasitic may cause oscillations [2]. Short-channel devices also struggle to maintain transconductance as drain current increases, complicating PA design [3]. Another challenge is the design of linear mixers with low voltage due to the scalability of the underlying technology [4]–[6]. The low breakdown voltage and considerable substrate loss of different technologies limit the PA [7]. Despite these limitations, a significant progress across different bands(V,Ka) has been done through CMOS and BiCMOS technologies utilizing Wilkinson power combining [8] and multi-stage LNA offers high gain and wideband coverage [9]. A dual-band PA operates using a tunable stub for band switching [10], while CMOS PA achieves also high gain with stable operation [11]. Conflicting performance requirements make PA design complex, requiring careful choices in device selection, biasing, topology, and load matching. To address the challenges, advanced amplifier topologies, adaptive biasing techniques, linearization methods, and the use of different technologies have been explored. These innovations contribute to addressing the critical trade-offs between performance parameters. In this paper, a two-stage Common Gate-Common Source (CG-CS) PA is designed using a superimposed staggered tuning approach, targeting a wireless telemetry system for patient monitoring and data transmission.

The architecture employs a Common-Gate (CG) input stage, which provides wideband input matching, followed

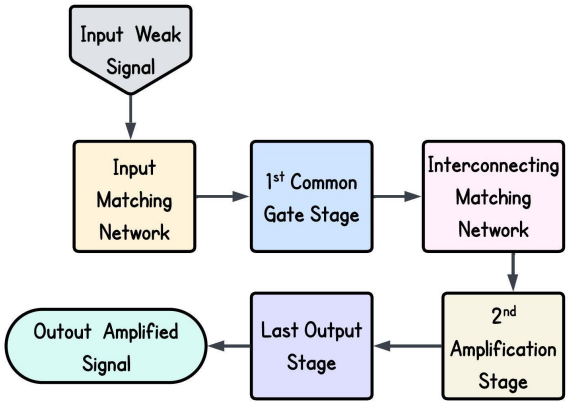


Fig. 4: Block diagram of proposed PA

by a Common-Source (CS) output stage that enhances gain. The configuration ensures dependable wireless data transfer between medical sensors and monitoring units. Fig.3 illustrates the design technique, where Fig.3(a) refers to sizing and biasing the amplifier based on analytical models and designer expertise to achieve the targets and Fig.3(b) shows those values are iteratively adjusted using simulation-based optimization tools until the specifications are met. By integrating a knowledge-driven, rule-based design with automated refinement, the methodology produces a robust initial design and delivers precise final optimization [12]. Fig.4 represents the typical structure of the proposed PA, where a weak signal is boosted through successive stages and delivers high power to the load effectively converting a small signal into strong output.

II. Methodology

A. Design of proposed PA

Even though subthreshold biasing provides higher ($\frac{g_m}{I_D}$) than strong inversion, wideband PA design becomes very difficult when analog and RF circuits operating in the subthreshold zone exhibit increased thermal noise, worse bandwidth, and poor linearity. When building a PA, several important factors (such as frequency range, gain, noise figure, input/output impedance, and power consumption) must be considered to ensure optimal performance. The suggested PA (shown in Fig.5) provides moderate bandwidth and modest gain. The operational frequency range of 0.9 GHz to 1.25 GHz is selected first. To make the design more suitable for the application needing flawless frequency performance and input impedance matching, a CG stage is employed in the first stage. Because of its high output impedance, low input impedance, enhanced frequency response, and efficient isolation between input and output stages, the CG circuit is preferred in PA designs. L_1 is used to match the amplifier to the 50 Ω source impedance.

A second amplification CS stage is typically added to the PA to boost gain. Because this stage helps to maintain

signal integrity and makes the amplifier suitable for several applications requiring broad frequency coverage. Additionally, it can boost the reflection coefficient, reduce distortion, and enhance overall performance, particularly in high-frequency applications where signal integrity is crucial. The second stage is added using staggered tuning to boost gain and bandwidth. The design illustrates the usage of L_5 and C_{gs2} to create a tank circuit at M_2's the source terminal. After that, an interstage matching T network is developed between the first and second stages. Finally, the buffer circuit is included, and the output-matching T network is added to improve the output return loss. A 50 Ω load impedance is matched utilizing the T network created by L_7, C_2 and C_3. M_5 allows the on-wafer characterization of PA using a 50 Ω-based setup. The bias voltage V_b of M_1 is biased at 0.83 V. Table$-I$ lists all key components used in the PA, along with their value, providing a clear overview of the circuit's design and the sizing of each element.

B. Schematic Diagram of PA

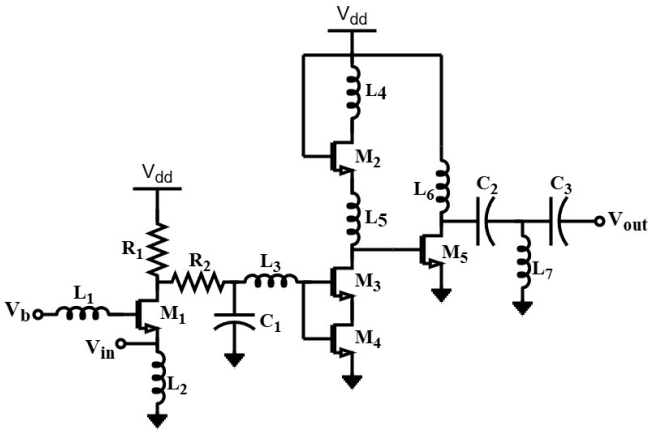


Fig. 5: Schematic of proposed wideband PA

III. PERFORMANCE ANALYSIS

PAs input matching is achieved by setting g_m. The small-signal equivalent circuit for the impedance calculation is shown in Fig.6. A CG input stage (Fig.6 a and c) serves as a current buffer with low input impedance and small Miller feedback, ideal for impedance matching and wideband operation. It drives a CS middle stage (Fig.6 b and d), which provides high voltage gain but its bandwidth is limited by Miller capacitance(C_{gd}). The cascade structure effectively combines current buffering and voltage amplification for achieving both wide bandwidth and significant gain.

A. Input Matching

Now, the impedance as perceived from the source terminal,

$$Z_{in} = j\omega(L_1 + L_2) + \frac{1}{j\omega C_{gs1}} + \frac{g_{m1L1}}{C} \tag{1}$$

TABLE I: Component Values for the PA

Aspect ratio	$\left(\frac{W}{L}\right)_{M1}$	$\left(\frac{W}{L}\right)_{M2}$	$\left(\frac{W}{L}\right)_{M3}$	$\left(\frac{W}{L}\right)_{M4}$
	$\frac{25\mu}{100n}$	$\frac{349.02\mu}{100n}$	$\frac{91\mu}{100n}$	$\frac{100\mu}{100n}$
	$\left(\frac{W}{L}\right)_{M5}$			
	$\frac{135\mu}{100n}$			
Inductor	L_1	L_2	L_3	L_4
	3	29.5	37	1.5
(nH)	L_5	L_6	L_7	
	115	110	91	
Capacitor	C_1	C_2	C_3	
(fF)	138	3.8×10^{15}	1.18×10^{5}	
Resistor	R_1	R_2		
(Ω)	7	30		

$$Z_{in2} = R_g \| j\omega L_3 \tag{2}$$

where, R_g is the gate resistance, g_{m1L1} is the transconductance of M_1, L_3 is the inductor at the input side of the 2nd stage, and $j\omega L_3$ represents the inductive reactance. At high frequencies, L_3 dominates, making Z_{in2} inductive. The output impedance at V_{out} depends on,

$$Z_{out} = ro_2 \| j\omega L_5 \tag{3}$$

where ro_2 is the output resistance of M_2, L_5 is the inductor connected to the drain. Since inductors have high impedance at high frequencies, Z_{out} is large, which is beneficial for power amplification.

B. Gain Analysis

Equation (4) emphasizes how important the network's Quality Factor (QF) is in connection to the amplifier's gain.

$$A_{v1} = (2\pi f_L) g_{m1} Q_1 \tag{4}$$

$$A_{v2} = g_{m3} \left(\frac{1}{\omega L_5} \| \frac{1}{g_{m5}} \right) \tag{5}$$

where $\left(\frac{1}{\omega L_5} \| \frac{1}{g_{m5}}\right)$ is the load impedance and the gain indicates a frequency-dependent voltage gain.

$$A_v = A_{v1} \times A_{v2} \tag{6}$$

QF is expressed in terms of conductance and LC,

$$Q_1 = \frac{\sqrt{L_1 + L_2}}{g_{m1} L_2} \tag{7}$$

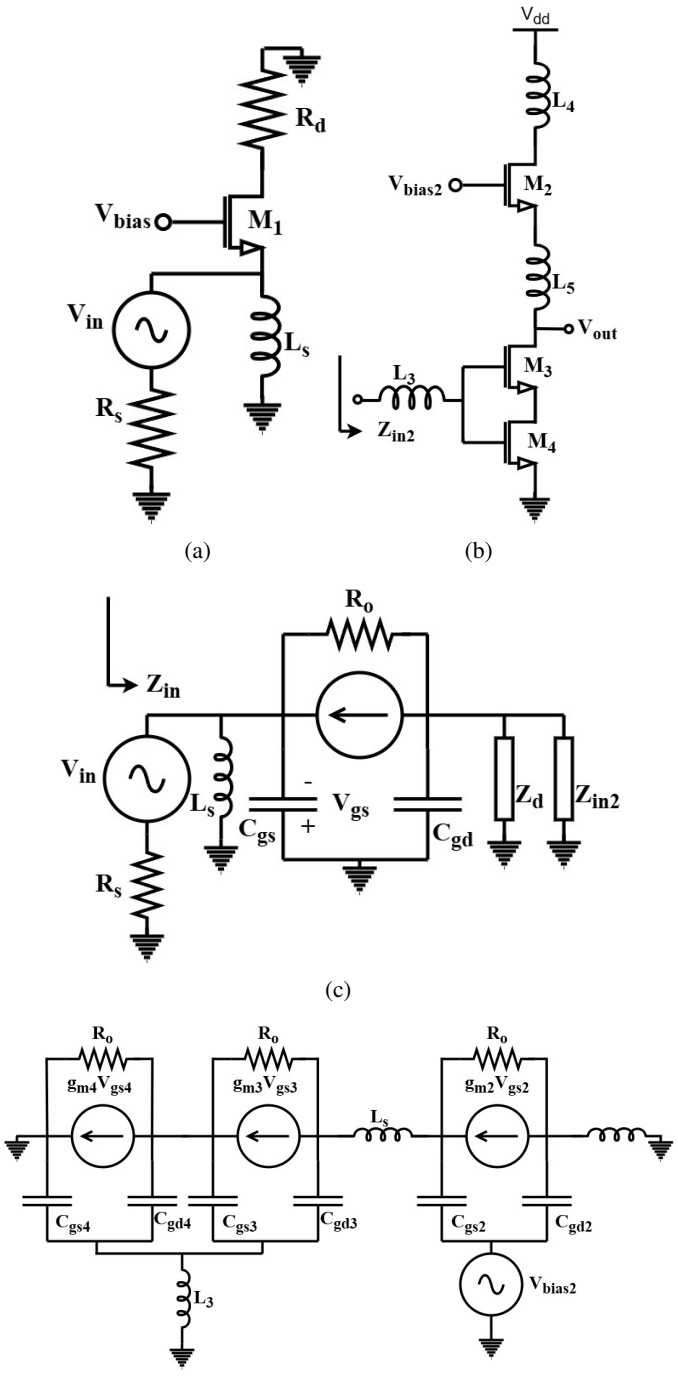


Fig. 6: (a) Configuration of a CG input stage, (b) Configuration of a CS middle stage, (c) Small signal of the CG stage, (d) Small signal of the CS stage

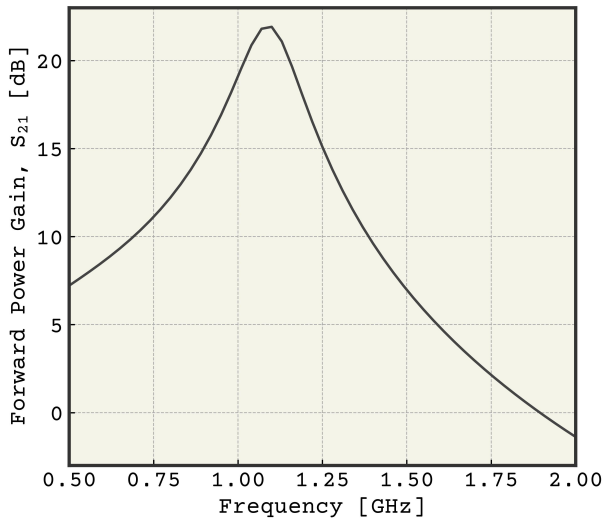
For Power Added Efficiency (PAE),

$$PAE = \left(\frac{P_{out} - P_{in}}{P_{DC}}\right) \tag{8}$$

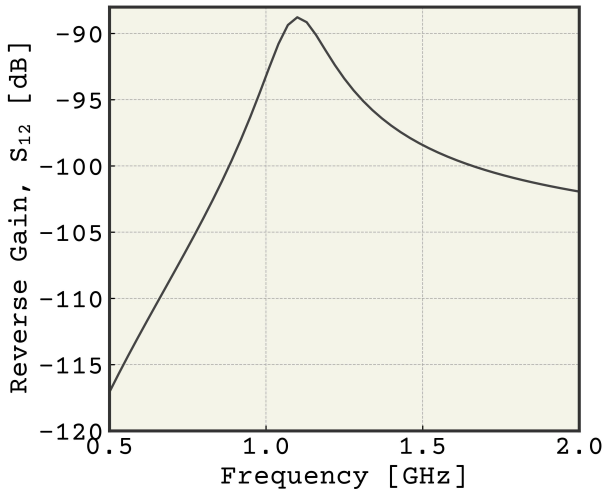
The circuit consists of the matching and amplifying elements of the network. The input matching network's components are L_1, L_2, and C_{gs1}. To adjust 2^{nd} stage to its resonant frequency, C_{gs2} and C_{gs3} are in conjunction with the inductor L_5. R_2, C_1, and L_3 are used to couple two stages. The output matching network makes the use of L_7, C_2, and C_3. The source and load impedance have been found to be $50\ \Omega$.

IV. Results and Discussions

The design simulations were performed using Spectre RF from the Cadence design suite. To ascertain the performance analysis, have to look at the SP analysis, which primarily



(a)



(b)

Fig. 7: (a) Forward gain, (b) Reverse gain of the proposed PA

shows the circuit's performance in a chosen location. The

parameters of the SP analysis, denoted as S_{11}, S_{21}, S_{12}, S_{22} and the k_f, B_1 factor allow to ascertain the circuit's stability factor and gain condition.

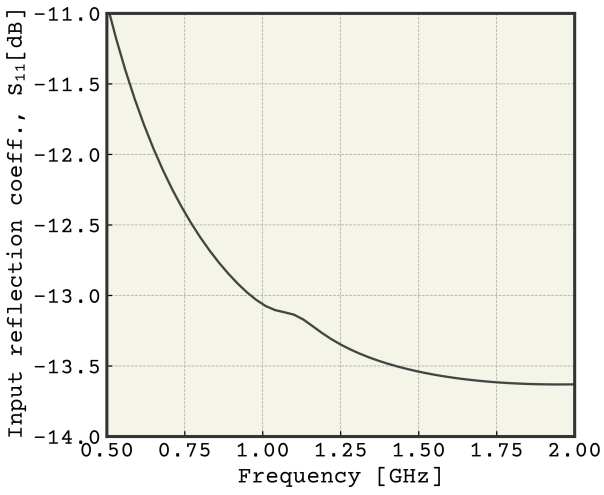
The gain curve and the isolation curve for the suggested PA simulations are both depicted in Fig.7(a)(b). The curves shows that if the frequency increases, the gain is peaking at 21.90 dB and reverse gain is -92 dB at the center frequency of 1.097 GHz. With a 1.2 V supply voltage, gain tapers to about 15 dB at the edges of the bandwidth. This gain value signifies that output power is more than hundred times amplified than input power. And the value of S_{12} means a little signal is leaking backward and the amplifier is doing a great job of blocking reverse signal flow. Adjusting C_1, L_3 and R_2, transconductance of the single stage is tuned without significantly affecting the other parameters. This allows for fine-tune the overall gain without negatively impacting other performance metrics.

TABLE II: Comparison Table

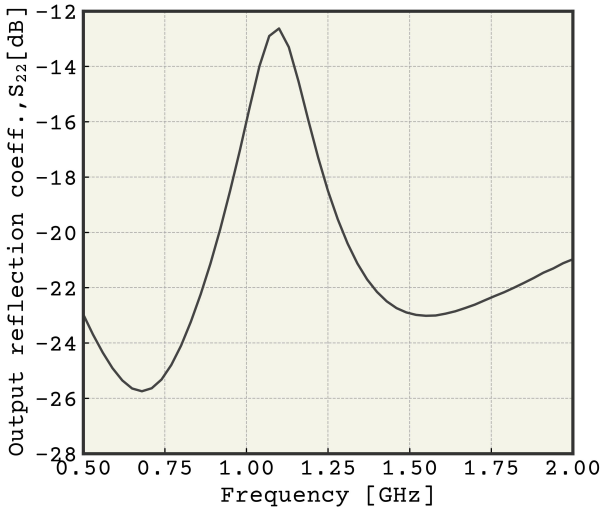
Ref.	[2]	[4]	[7]	[11]	This work
Tech. (nm)	–	180	90	180	90
Supply Voltage (V)	4	1.8	1.1	1.8	1.2
Gain (dB)	17.2	10	9.56	21.3	21.90
Bandwidth (MHz)	2050	At 2400	–	100000	350
S_{11}(dB)	-10|-17	-10	–	–	-13.14
S_{22}(dB)	-10|-28			–	-12.66

The simulation results for the suggested PA are shown in Fig.8(a)(b), depicting both the input reflection coefficient (S_{11}) and output reflection coefficient (S_{22}) curves. Here the whole bandwidth is maintained below -10 dB for both S_{11} and S_{22}, suggesting a good matching of the input and output. It indicates that most of the power is entered into the amplifier and delivered to the load and ensures minimum power loss. At the operating point, the input and output return losses are found to be -13.14 dB and -12.66 dB, respectively, where the reverse gain is - 88.84 dB. At the lower feet of bandwidth (0.9 GHz), these (S_{11}, S_{22}, S_{12}) values are -12.87 dB, -20.71 dB and -99.08 dB respectively and for the higher feet (1.25 GHz), they are -13.35 dB, -18.50 dB, and -93.4 dB.

Over this bandwidth, both the stability factor, k_f an $B_1 f$ follow the condition of a stable circuit. At the operating point, the value of Rollet's stability factor (k_f) has been found to be 1kdB $>$ 1. It implies that the designed circuit is unconditionally stable as shown in Fig.9. The Bodway stability factor has been found to be 0.992 dB. The non-zero and positive value indicates better stability characteristics in Fig.10. So the designed PA is stable.



(a)



(b)

Fig. 8: (a) Input reflection co-efficient, (b) Output reflection co-efficient of the proposed PA

The values of P_{out}, P_{in}, P_{DC} have been found 1.318 μW, 0.914 μW, and 1.993 μW respectively, from the calculator tools of Cadence software. These reflect the linearized bias condition. PAE of 20.27 percent is found by (8) of this PA, which indicates the telemetry system operates at low power.

After performing a transient analysis in Cadence ADE to generate power waveform data over time, instantaneous power is calculated using the calculator tool. By applying the average function, an average power consumption of 153.1 mW is obtained.

The proposed PA's performance is outlined in Table$-II$, which compares the circuit with the reference work in terms of gain, bandwidth and impedance matching. It highlights the improvement and shows that the amplifier is competitive with or superior to contemporary implementations.

This combination of low power consumption, wideband

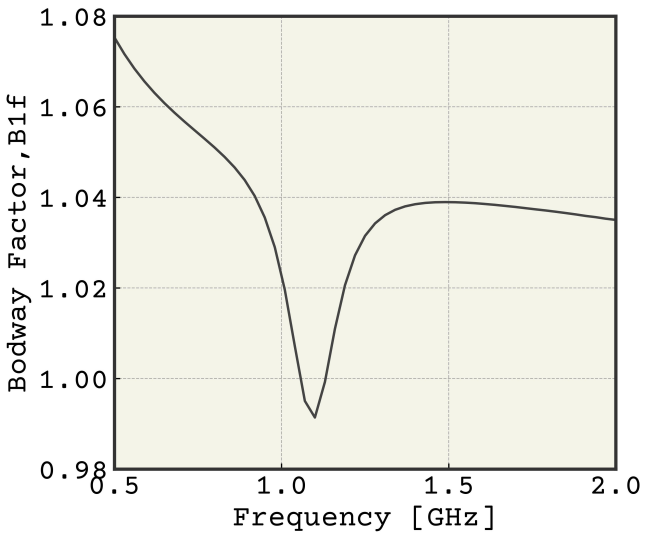


Fig. 9: Bodway (B_1f) stability factor the proposed PA

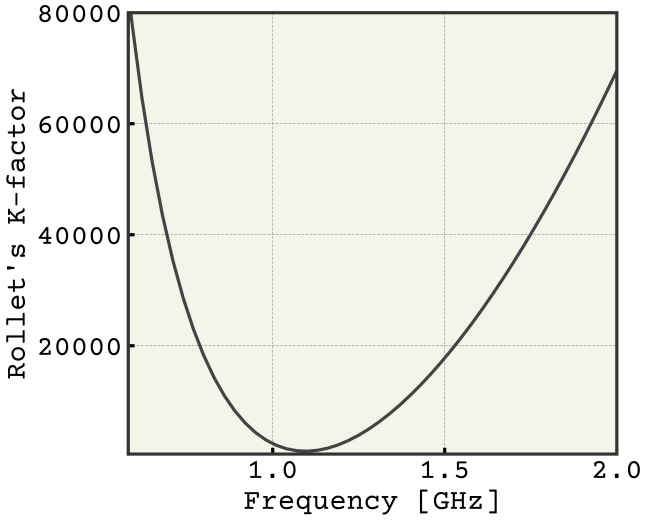


Fig. 10: Rollet's stability factor (k_f) of the proposed PA

performance, robust gain, and assured stability makes this amplifier an ideal for compact, reliable biomedical wearables or implants. Typically, such devices require low power and high reliability to ensure patient safety, minimize heat dissipation and prolong battery life. The amplifier's stable performance supports continuous, real-time data transmission of vital signs without bulky hardware—crucial for modern healthcare solutions.

V. Conclusion

In conclusion, the study looked at PA design and optimization for higher gain and bandwidth in the 0.9 GHz to 1.25 GHz frequency range. The first single-stage PA design had a lower gain and had trouble matching input impedance because of frequency-dependent transconductance and parasitic capacitance. However, the cascaded PA shows better gain performance at a lower frequency by incorporating a second stage. To enhance impedance matching and produce greater gain and reduced return loss, matching networks were also incorporated into the design. The PA's gain, bandwidth, and matching performance were all successfully increased by the optimization efforts, meeting the necessary goals.

References

[1] HK Yogitha, K Sinchana, Shristi Biyani, and Rashmi Seethur. Design of a 90nm instrumentation amplifier for high precision signal acquisition applications. In *2023 IEEE 9th International Conference on Smart Instrumentation, Measurement and Applications (ICSIMA)*, pages 116–120. IEEE, 2023.

[2] Mohamed Ribate, Rachid Mandry, Jamal Zbitou, Larbi El Abdellaoui, Ahmed Errkik, and Mohamed Latrach. 1.25 ghz–3.3 ghz broadband solid state power amplifier for l and s bands applications. *International Journal of Electrical and Computer Engineering*, 9(5):3633, 2019.

[3] Esmaeil Ranjbar Koleibi, Maher Benhouria, Konin Koua, William Lemaire, Sébastien Roy, and Réjean Fontaine. A low-power low-noise biopotential amplifier in 28 nm cmos. In *2022 20th IEEE Interregional NEWCAS Conference (NEWCAS)*, pages 143–147. IEEE, 2022.

[4] Wei Cai, Liang Huang, WuJie Wen, and Hang Zhou. Low power class ab si power amplifier for wireless medical sensor network. *International Journal of Biomedical Engineering (IJBE)*, 1(1), 2018.

[5] Jingzhou Pang, Yue Li, Meng Li, Yikang Zhang, Xin Yu Zhou, Zhijiang Dai, and Anding Zhu. Analysis and design of highly efficient wideband rf-input sequential load modulated balanced power amplifier. *IEEE transactions on microwave theory and techniques*, 68(5):1741–1753, 2020.

[6] Chien-Chih Lin, Chun-Han Yu, Hsin-Chih Kuo, and Huey-Ru Chuang. Design of 60-ghz 90-nm cmos balanced power amplifier with miniaturized quadrature hybrids. In *2014 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*, pages 52–54. IEEE, 2014.

[7] Nan Zhang, Lingling Sun, Jincai Wen, Jun Liu, Jia Lou, Guodong Su, and He Li. A 60ghz power amplifier using 90-nm rf-cmos technology. In *2011 9th IEEE International Conference on ASIC*, pages 933–936. IEEE, 2011.

[8] A Hamidian, V Subramanian, R Doerner, R Shu, A Malignaggi, MK Ali, and G Boeck. 60 ghz power amplifier utilizing 90 nm cmos technology. In *2011 IEEE International Symposium on Radio-Frequency Integration Technology*, pages 73–76. IEEE, 2011.

[9] R Sananes and E Socher. 52–75 ghz wideband low-noise amplifier in 90 nm cmos technology. *Electronics letters*, 48(2):71–72, 2012.

[10] Asad Ali Nawaz, John D Albrecht, and Ahmet Cagri Ulusoy. A 28/60 ghz dual-band power amplifier. In *2019 IEEE MTT-S International Microwave Symposium (IMS)*, pages 630–633. IEEE, 2019.

[11] Damandeep Singh. Power amplifier for 100ghz frequency in 180nm cmos technology. 2015.

[12] Divya Sharma and Vijay Nath. Cmos operational amplifier design for industrial and biopotential applications: Comprehensive review and circuit implementation. *Results in Engineering*, page 102357, 2024.