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Design of a Multi-Stage Common Source LNA with Enhanced Gain and Noise Performance for SIGINT Applications

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***Abstract*—This paper proposes a multi-stage common-source Low Noise Amplifier(LNA) that achieves high gain and superior energy efficiency, utilizing 90 nm CMOS technology. The application of LNA in SIGINT systems has drawn significant interest due to its effectiveness in amplifying weak signals while minimizing external noise. Achieving a low noise figure while preserving low power consumption is a major challenge in LNA design for portable systems. With a supply voltage of 1.2 V, the proposed LNA achieves a noise figure(NF_{min}) of 6.21 dB and a power gain of 34.43 dB over the frequency range of 7.069 GHz to 7.4558 GHz. It ensures the maximum output power transmission to a 50 Ω load by having a strong impedance matching of S_{11} < -11.907 dB and S_{22} < -9.04 dB. At the operating frequency of 7.243 GHz, the S-Parameters are S_{11} = -12.43 dB, S_{22}= -15.11 dB, and S_{12} = -88.9885 dB, and the power consumption is 69.33 mW. The LNA is stable as $Kf > 1$ and $B1f > 0$, which meets the desired specifications.**

***Index Terms*—CMOS, Common Source LNA, Impedance matching, Gain, SIGINT.**

I. Introduction

An LNA is the first active component for improving, detecting and analyzing hostile signals prior to generating appropriate jamming responses in a jamming and signals intelligence(SIGINT) system. LNAs are mainly used for amplification of the desired signals received by the antenna with minimum noise, power consumption, and distortion. Therefore, an LNA should be designed to achieve high gain and minimum noise to enhance the sensitivity and reliability of SIGINT systems. LNAs enable accurate and effective jamming by assisting in determining the frequency and features of adversary signals. As shown in Fig.1, the SIGINT system includes several key components and the signal flows from antenna to DSP through filter, LNA, Mixer and LO, IF amplifier.

These circuits have recently gained significant attention with CMOS technology providing the necessary gain to overcome noise and power dissipation. The performance of LNAs is influenced by process technologies and circuit topologies.

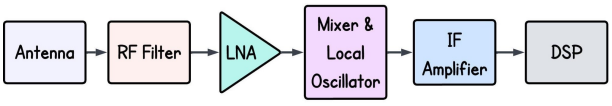

Fig. 1: Block Diagram of a SIGNIT Receiver Front-End

While designing LNAs with different topologies for performance analysis, key challenges include impedance matching for optimal power transfer, the requirement for a higher supply voltage, and degraded noise performance [1]. It may limit suitability in low-power or high-performance applications [2]. The common-source(CS) configuration is preferred for its excellent balance between performance, simplicity, scalability and CMOS compatibility with source degeneration.

Using 90 nm CMOS technology, channel-length scaling in VLSI has reached the nanometer range, pushing the MOSFET transit frequency (f_t) into the gigahertz region. The component supports performance along with topologies but does not prioritize all performance criteria equally. As a result, compromise may be necessary. The challenges motivate RF architecture exploration, balancing linearity, input matching, and power dissipation [3]. Recent efforts have focused on improving LNA linearity, stability, and noise performance [4]. Good gain, little NF, unconditional stability, and low power dissipation are characteristics of an ideal narrow band LNA [5]. CMOS has emerged as a viable technology like Silterra (nm,μm) for mixed-signal/RF system-on-chip due to the continuous scaling of channel-lengths [6]–[8]. In parallel, improvements in substrate integrated waveguide structure have been introduced to enhance quality factor for better RF performance [9].Variable gain designs to ultra-broadband LNAs spanning a wide frequency range demonstrate versatility by enabling low-noise, high-gain operation across diverse wave applications [10], [11]. A single-stage common source LNA(CS-LNA) offers a simple design but suffers from limited gain, potential stability issues, and suboptimal noise performance for SIGINT

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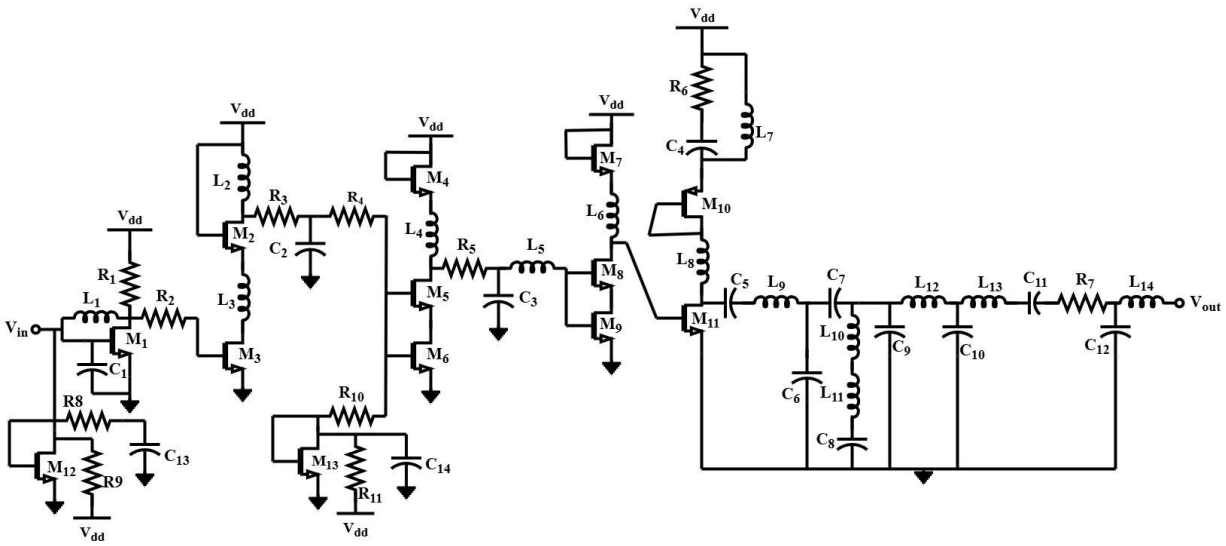

Fig. 2: Schematic Diagram of the proposed LNA

systems. However, multi-stage CS-LNA could be explored to provide greater design flexibility in tuning, better control over impedance matching, signal integrity, sensitivity, and stability. It can be implemented efficiently in terms of area and power.

In this paper, a multi-stage CS-LNA configuration is used due to its superior noise performance. An RF input signal is pre-amplified by the input-matching series network. To increase stability and control gain, the input signal is applied to the gate, the output is taken from the drain, and the source is connected to a tiny impedance or ground to efficiently amplify signals.

In this study, the LNA is intended for use in SIGINT with the frequency band being 386.8 MHz using 90 nm CMOS technology. The simulation is carried out using Cadence Virtuoso software. This paper presents a multi-stage configuration of CS-LNA. The design of the proposed LNA is briefly described in Section II, the performance analysis of LNA is presented in Section III, the simulation results obtained are shown in Section IV and the conclusion is reported in Section V.

II. METHODOLOGY

A. Design of LNA

An LNA amplifies weak signals with minimal signal-to-noise ratio(SNR) degradation by optimizing components, operating points, and circuit topologies while balancing power gain and impedance matching. It can be designed using different topologies and the LNA's parameters vary accordingly. Our LNA's structure is shown in Fig.2. which depicts a 5-stage LNA.

The first stage is the CS stage with a resistive load. A basic amplifier setup that uses a MOSFET (or JFET), is a CS stage with a resistive load. Because of its capacity to generate voltage gain, it is frequently utilized in analog circuits. In an NMOS CS stage, the MOSFET operates with the input signal applied at the gate. Its main advantages are simple design, moderate voltage gain, and ease of implementation. The 2nd, 3rd, 4th, and 5th stages are CS stages with an inductive load, where M_5, M_{11} and M_8 are the main operating amplification transistors.

L_4 and L_6 are used as a load to provide higher gain and efficiency at higher frequencies as sometimes resistor load leads to a trade-off between voltage gain and the supply voltage and makes it difficult to scale down. So this circuit can operate at low supply voltage. L_8 serves as a source-degeneration inductor. L_7 (along with R_6 and C_4) is part of the biasing network. M_4, M_7 and M_{10} act as cascade devices for improving performance and M_6 and M_9 serve as active loads at the source of M_5 and M_8. 3rd and 1st stages are separately biased by the MOSFET resistor diode. Capacitors and inductors are used to couple the output, creating an impedance-matching network with the last stage for matching purposes. The 2nd, 3rd, and 3rd, 4th stages are interconnected by T topology. The output matching network is composed of T, L, and π network.

B. Schematic Diagram of the proposed LNA

The schematic of the multi-stage CS-LNA is shown in Fig.2. The M_1 transistor's size was selected to have a sufficient g_m that demonstrates input power matching. The LNA's input impedance can be computed using the following formula (1) :

$$Z_{in} = \frac{1}{g_{m1}} + j\omega C_{gs} \tag{1}$$

$$Z_{out} = j\omega L_{out} \| R_L \tag{2}$$

The 2nd, 3rd, and 4th CS stages collectively function as an active noise-canceling stage by exploiting the phase relationship between signal and noise. The noise voltage from transistors M_3, M_5, and M_8 exhibits an out-of-phase behavior at the inputs of these stages, enabling destructive interference that reduces noise voltages through the feedforward noise-cancellation principle. Meanwhile, the in-phase signal components from the previous stage are constructively combined at the output node, preserving the desired signal strength. This approach benefits from the inherent wideband response, low parasitic capacitance, and low noise figure(NF) of the CS stages, contributing to the high overall gain and noise reduction. Finally, transistor biasing is accomplished via current mirror circuits. A 101.8 fF capacitor is placed between the gate and the ground line to ensure correct AC grounding and to filter out the generated noise by the biasing circuit. Table$-I$ lists the suggested LNA's components value.

Here, 7.243 GHz denotes the center frequency of the input signal, while bandwidth 387 MHz defines the frequency range over which the LNA sustains acceptable gain and noise figure.

III. PERFORMANCE ANALYSIS

This circuit is a Multi-Stage CS Amplifier with Inductive Loads and Impedance Matching, commonly used in RF front-end applications like LNAs or Power Amplifiers(PAs). To maximize gain, minimize NF, and achieve proper impedance matching, several cascaded CS stages, current mirror biasing, and LC matching networks are used.

A. Gain Analysis

Each stage follows CS topology with inductive load, where the small-signal gain is given by:

$$A_v = -g_m(Z_{Load} \| Z_{out}) \tag{3}$$

where g_m = the transconductance of MOSFET, Z_{Load} = the equivalent impedance, Z_{out} = the next stage's impedance. For 1st and 2nd stage, L_1, L_2, C_1 provide the optimal power transfer and for them, following (3) the gain would be

$$A_{v1} = -g_{m1}(j\omega L_3 \| Z_{in2}) \tag{4}$$

For 3rd stage,

$$A_{v2} = -g_{m4}(j\omega L_5 \| Z_{in3}) \tag{5}$$

For 4th stage,

$$A_{v3} = -g_{m7}(j\omega L_7 \| Z_{in4}) \tag{6}$$

For 5th stage,

$$A_{v4} = -g_{m10}(j\omega L_8 \| Z_{match}) \tag{7}$$

Total gain,

$$A_v = A_{v1}.A_{v2}.A_{v3}.A_{v4} \tag{8}$$

Using (1) and (2) impedance value can be achieved. The matching network (L_{14}, C_{12} etc.) adjusts Z_{out} to the required value (50Ω).

TABLE I: Components Value

MOSFET (μm)					
$\mathbf{M}_1$	0.4	$\mathbf{M}_6$	15.995	$\mathbf{M}_{11}$	24
$\mathbf{M}_2$	120	$\mathbf{M}_7$	50.64	$\mathbf{M}_{12}$	7.5
$\mathbf{M}_3$	56.67	$\mathbf{M}_8$	39.75	$\mathbf{M}_{13}$	5
$\mathbf{M}_4$	110.64	$\mathbf{M}_9$	15.995		
$\mathbf{M}_5$	39.50	$\mathbf{M}_{10}$	150		
Capacitor (fF)					
$\mathbf{C}_1$	142.46	$\mathbf{C}_6$	4.46	$\mathbf{C}_{11}$	80
$\mathbf{C}_2$	1.80	$\mathbf{C}_7$	45	$\mathbf{C}_{12}$	19.80
$\mathbf{C}_3$	1.80	$\mathbf{C}_8$	4	$\mathbf{C}_{13}$	101.80
$\mathbf{C}_4$	1×10^5	$\mathbf{C}_9$	10	$\mathbf{C}_{14}$	101.80
$\mathbf{C}_5$	60	$\mathbf{C}_{10}$	10		
Resistor (Ω)					
$\mathbf{R}_1$	15	$\mathbf{R}_6$	150	$\mathbf{R}_{11}$	1×10^3
$\mathbf{R}_2$	1	$\mathbf{R}_7$	5		
$\mathbf{R}_3$	13	$\mathbf{R}_8$	55		
$\mathbf{R}_4$	15	$\mathbf{R}_9$	950		
$\mathbf{R}_5$	13	$\mathbf{R}_{10}$	3.5×10^3		
Inductor (nH)					
$\mathbf{L}_1$	1×10^{-3}	$\mathbf{L}_6$	5	$\mathbf{L}_{11}$	0.5
$\mathbf{L}_2$	5.3	$\mathbf{L}_7$	1	$\mathbf{L}_{12}$	10
$\mathbf{L}_3$	3.5	$\mathbf{L}_8$	0.83	$\mathbf{L}_{13}$	1.03
$\mathbf{L}_4$	5	$\mathbf{L}_9$	10	$\mathbf{L}_{14}$	0.90
$\mathbf{L}_5$	0.3	$\mathbf{L}_{10}$	0.5		

B. Noise Analysis

The NF measures how much noise the amplifier adds. It can be determined from the following equation,

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{A_{v1}} + \frac{NF_3 - 1}{A_{v1}.A_{v2}} + ... \tag{9}$$

$$F = 1 + \frac{\gamma}{\alpha} + 4\frac{R_s}{R_L} \tag{10}$$

$$NF = 10\log(F) \tag{11}$$

Where, F = Noise factor, γ = the excess channel thermal noise coefficient, and α = the ratio between g_{m1} and the zero bias drain conductance gd_{o1}, R_s = input resistance, and R_L = load resistance.

C. Stability Analysis

A source degeneration inductor L_8 is used here to improve the stability. Cascaded configuration improves isolation by

increasing Kf and inductive load L_5 can create resonances. L_{14} and C_{12} prevent reflection. The Rollet's stability factor (kf) is

$$Kf = \frac{(1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2)}{2|S_{12}.S_{21}|} \tag{12}$$

Another metric used to determine the stability is B_1f, which follows (13)

$$B1f = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{13}$$

As the value of Kf >1 which is shown in Fig.5 and B_1f > 0 which is shown in Fig.6, so the designed circuit is stable.

IV. Results and Discussions

Cadence Virtuoso software is used to simulate the proposed design. The suggested design's bandwidth is 386.8 MHz (7.069 GHz to 7.4558 GHz). Over this bandwidth the input reflection coefficient and output reflection coefficient are shown in Fig.3, and Fig.4, respectively. Throughout the entire bandwidth, both S_{11} and S_{22} are maintained at $<$ - 9 dB. It indicates that the most of the power is entering the amplifier and being transmitted forward to the next stage and a small amount of power is reflected back. It also means minimal power loss. So, the LNA has a well-matched input and output across the bandwidth.

Here, we observed that the maximum input and output impedance matching values at 7.243 GHz are -12.43 dB and -15.11 dB, respectively. Fig.5 shows the gain curve for the proposed LNA simulation. The gain increases with frequency. Around 34.369 dB, 32 dB, and 32.0454 dB are the gains at 7.069 GHz, 7.243 GHz, and 7.4558 GHz, respectively. This larger gain value shows that output power is more than hundred times larger than the input power, indicating better amplification. Fig.6 shows the improved isolation of the circuit. The value of S_{12} at the operating point is almost -92 dB which means a little signal is leaking backward and the amplifier is doing a great job of blocking reverse signal flow.

Effective tuning of the LNA's overall gain is possible by varying R_9 and R_{11}, which adjusts the single stage's transconductance without significantly altering the other parameters. When the LNA requires a specific gain value, this feature makes it simpler to alter the design. The noise performance of the proposed architecture is shown in Fig.7. The lowest noise level at 7.069 GHz is around 6.26 dB. It varies between higher and lower frequencies. The highest noise level is 6.21 dB at 7.4558 GHz. Although the value is moderate for ultra-low noise amplifiers, the design is ideal for portable SIGINT systems, where high gain, low power, energy efficiency and integration are prioritized over a marginally higher noise figure.

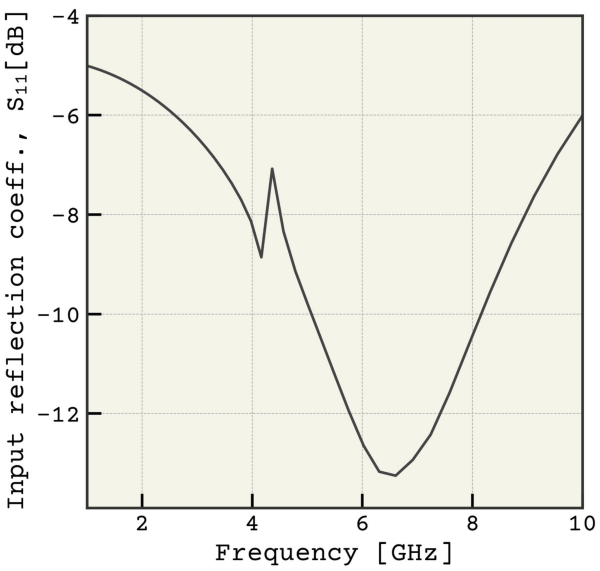

Fig. 3: Input Reflection co-efficient of the proposed LNA

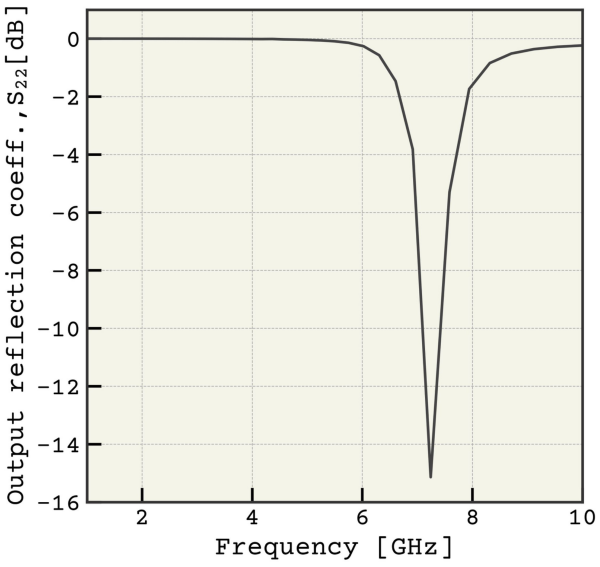

Fig. 4: Output Reflection co-efficient of the proposed LNA

Over this bandwidth, both the stability factor, kf and $B1f$ satisfy the condition of a stable circuit. At the operating point, the value of Rollet's stability factor (kf) = 243.551 $>$ 1, and Bodway's stability factor = 1.0211 $>$ 0 (shown in FIg.8 and Fig.9), implying that the designed circuit LNA is stable. The proposed CMOS LNA's performance is outlined in Table $-II$, which compares the circuit with the reference work.

After conducting transient analysis in Cadence, the power consumption of the circuit was calculated using the calculator tool and found to be 69.33 mW.

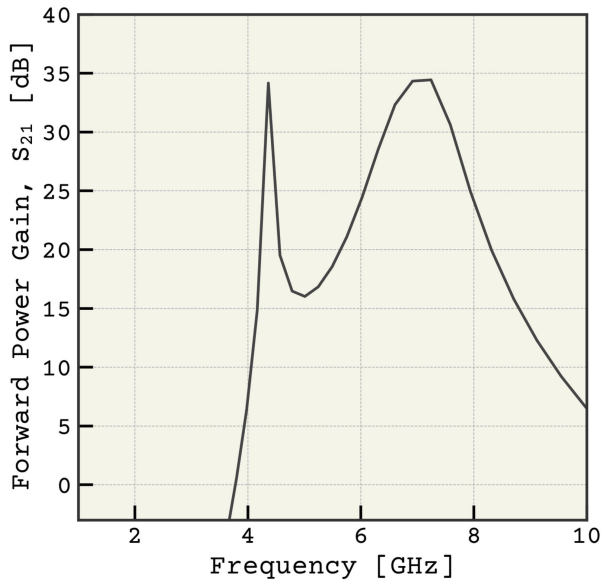

Fig. 5: Input transmission co-efficient (Gain) of the proposed LNA

The LNA reduces transmission losses and improves input-output isolation. Additionally, some geometrical characteristics of it help to increase S_{11} and S_{22}. Multi-CS stage's topological characteristics allow dispersed components to function over a bandwidth.

While simulation results show promise, real-world typical CMOS designs may encounter issues like process variation, parasitic effects, and device mismatch, which can adversely affect the performance. Such challenges can be mitigated

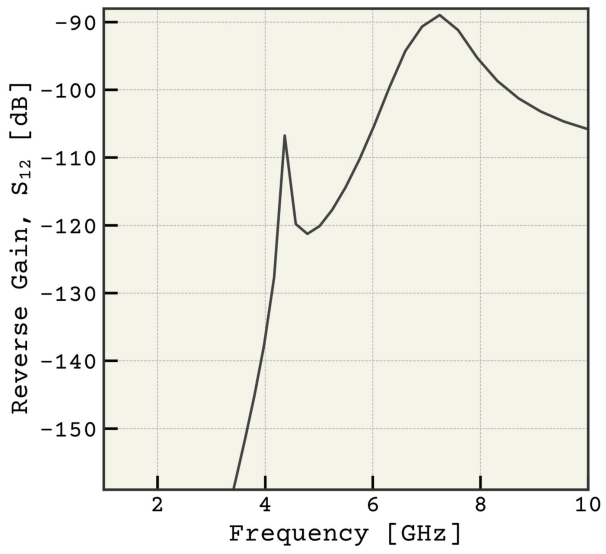

Fig. 6: Output transmission co-efficient (Isolation) of the proposed LNA

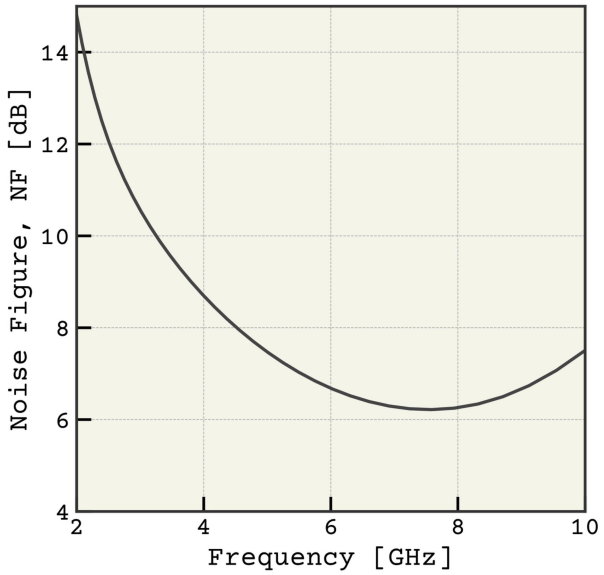

Fig. 7: Noise Figure of the proposed LNA

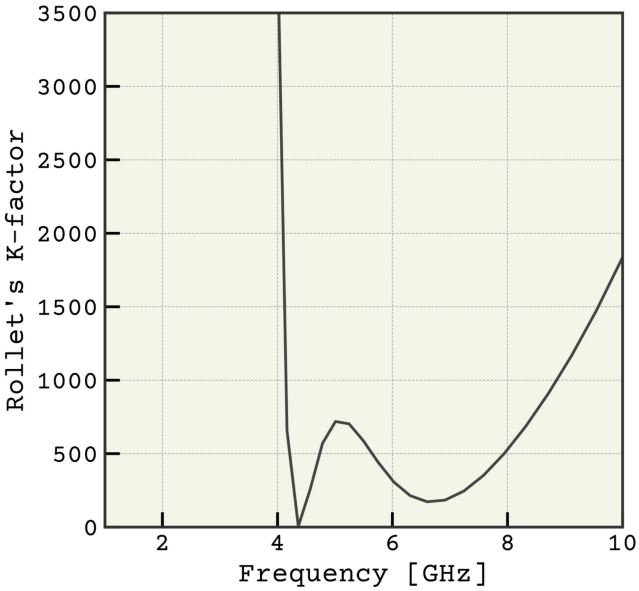

Fig. 8: Rollet's stability factor (k_f) of the proposed PA

through incorporating robust layout, shielding, and calibration. The proposed CMOS design utilizes multi-stage common-source architecture with simple biasing makes it well-suited for standard CMOS integration.

So, the designed LNA is not only theoretically sound but also promising for practical SIGINT applications, especially in systems where low noise and moderate gain in the MHz range are critical.

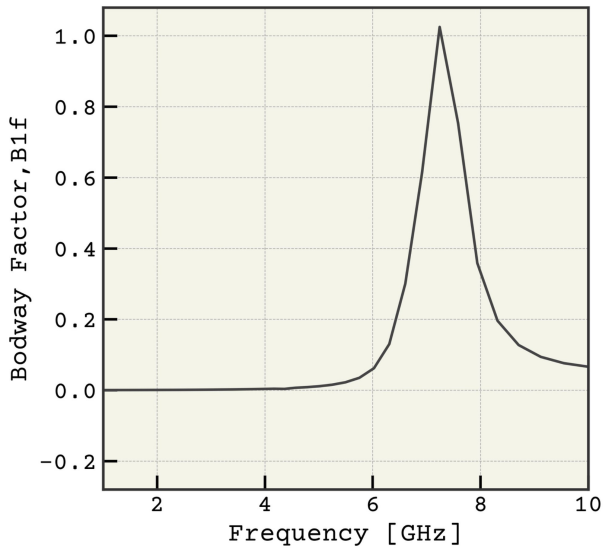

Fig. 9: Bodway (B_1f) stability factor the proposed LNA

TABLE II: Comparison Table

Ref.	[9]	[10]	[11]	This work
Frequency (GHz)	69	57-64	140-220	7.243
CMOS Tech. (nm)	180	-	-	90
Bandwidth (GHz)	4.5	7	80	0.387
Supply Voltage (V)	1.8	1.8	-	1.2
Topology	1-Stage	-	-	Multi-Stage CS
Power Gain (dB)	9.75	20-30	15.5	34.43
NF (dB)	8.33	6	6.9,6.1,8.2	6.22

V. Conclusion

This paper presented the design of a multi-stage common-source LNA using 90 nm technology whose cascaded LNA stages achieve a noise figure of 6.21 dB and a gain of 34.43 dB across 386.8 MHz, with a low supply voltage. Despite multiple stages, the design reduces the transmission losses, enhances better isolation between input and output, and maintains moderate noise levels and low power consumption. Comparing the simulation results of the integrated CMOS multi-stage LNA with previous studies, it can be concluded that this design marks a significant step toward the advancement of single-chip receiver development for SIGINT systems.

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